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EXAMINER
HOYE, MICHAEL W

ART UNIT	PAPER NUMBER
2614	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/398,913	KLEBANOV ET AL.	
	Examiner	Art Unit	
	Michael W. Hoye	2614	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *2/12/03* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *2-13,22 and 23* is/are allowed.

6)☒ Claim(s) *14-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *9/14/99 (Fig. 2)* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *12 February 2003* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed on 2/12/03 with respect to claims 14, and 18-20 have been fully considered but they are not persuasive.

2. Regarding claim 14, the applicants argue, "the examiner's citation to Chauvel, col. 8, lines 45-47, as teaching a transport stream having data signals and control signals" is improper, and further, "contest the examiner's citation to Chauvel, Col. 9, lines 11-13, as teaching the reception of a transport stream associated with a digital video broadcast signal, the transport stream having data signals and *control signals* as taught by the applicants."

In response, the examiner respectfully disagrees with the applicant. First, col. 8, lines 45-47, of Chauvel discloses receiving a broadcast signal which the user has selected and a circuit for recovering the digital data in the selected signal. Chauvel further discloses in col. 8, lines 63-65, that, "the clock is adjusted to be synchronized with the clock signals found in the received digital data." Therefore, the clock synchronization signals or "control signals" are included in the digital data that is received. Furthermore, col. 9, lines 11-13, of Chauvel disclose MPEG-2 audio and video decoders for receiving MPEG-2 audio and video transport streams associated with digital video broadcast signals (also see col. 3, lines 35-38 for MPEG standard). Chauvel clearly teaches receiving a transport stream associated with a digital video broadcast signal, the broadcast signal having data signals and control signals.

Continuing with claim 14, the applicants also argue that, "the traffic controller element of Fig. 1B fails to disclose the claimed step of generating a secondary set of control signals from the transport stream control signals as taught in the applicants Specification."

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., generating a secondary set of control signals, such as a Start of Field (SOF) signal, a Start of Active (SOA), and End of Active (EOA) signal, a Data Active (DACTIVE) signal, and a Video Data (VDATA) signal) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

In further response the examiner also cites col. 12, lines 15-28, of Chauvel, in reference to the traffic controller 310 and circuit 200, where PACCLK high signals valid packet data and DERROR is used to indicate a packet that has data errors.

Continuing with claim 14, the applicants also argue that, "the memory interface and buffer of Chauvel's Figure 18B (Elements 313 and 312a, respectively) do not appear to teach the applicant's claimed step of storing at least a portion of the transport stream data signals in a memory buffer *controlled by the secondary set of control signals...*"

In response, the examiner respectfully disagrees with the applicant. In col. 10, lines 12-40, Chauvel discloses that, "The Transport Packet Parser (TPP) 210 in the circuit 200 processes the header of each packet and determines whether the packet should be discarded, further processed by ARM CPU 220, or if the packet contains relevant data and may be stored without any intervention from the ARM 220. The TPP 210 sends all packets requiring further processing

or containing relevant data to the internal RAM 240 via the traffic controller (TC) 310...The data transfer from TPP 210 to SDRAM 312 is done via DMA [Direct Memory Access] set up by the traffic controller (TC) 310...The traffic controller 310 repacks the data and gets rid of the voids created by any header removal." Also, see Figs. 1B and 18B, where control signals indicated by the arrow between the traffic controller 310 and memory interface 313 indicate the claimed secondary set of control signals, and see col. 18, line 66 – col. 19, line 12, with reference to the traffic controller authorizing and managing DMA transfers, memory access, data transfers, etc... Therefore, the traffic controller 310 is directly involved in storing at least a portion of the transport stream data signals in a memory buffer (312/312a, in Fig. 18B) *controlled by the secondary set of control signals* (which are output from the traffic controller 310 to the memory interface 313.

3. Regarding claims 18-20, the applicants argue, "the TPP *discards packets not selected by an application and routes as many packets as possible* without real-time help from either the ARM CPU 220 or software running on the ARM CPU..." and that, "such a device is not required in the applicants' claim 18."

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., the video graphics adapter as illustrated in applicants' Figures 2, 4 and 5) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

4. Applicant's arguments, see Amendment A in the **REMARKS** section, specifically, on page 28, line 29 – page 29, line 6, filed 2/12/03, with respect to new claim 22 (based on canceled independent claim 1) have been fully considered and are persuasive. The rejection of independent claim 1 (now new claim 22) has been withdrawn. Moreover, the rejection of dependent claims 2-13 and new claim 23 are withdrawn, see Amendment A in the **REMARKS** section, page 29, line 5 – page 32, line 2, filed 2/12/03.

5. Applicant's arguments with respect to claim 15-17 have been considered but are moot in view of the new ground(s) of rejection.

6. Applicant's arguments with respect to claim 21 have been considered but are moot in view of the new ground(s) of rejection.

Drawings

7. The drawings are objected to because the DVB (Digital Video Broadcast) label as shown in Fig. 2 also contains the label (ANALOG). The two apparently contradictory labels should not appear together since the signal is either digital or analog. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

8. Claim 21 is objected to because of the following informalities: in lines 3 and 6 of the claim the wording "of frame buffer memory" is unclear as to whether or not there is a single frame buffer memory or more than one frame buffer memory. If the claim is referring to a single frame buffer memory the claim language should be amended to read --of the frame buffer memory-- in lines 3 and 6 respectively. Appropriate correction is required.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

10. Claims 14, and 18-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Chauvel et al (USPN 6,369,855).

As to claim 14, the Chauvel et al reference discloses a method for receiving video graphics data comprising the steps of receiving a transport stream (as shown in Figure 1B by the Transport Data input), associated with a digital video broadcast signal (Digital Satellite System (DSS) - col. 9, lines 41-42 & col. 11, lines 1-2), the transport stream having data signals and control signals which is met by col. 8, lines 45-47, of Chauvel, that discloses receiving a broadcast signal which the user has selected and a circuit for recovering the digital data in the selected signal. Chauvel further discloses in col. 8, lines 63-65, that, "the clock is adjusted to be synchronized with the clock signals found in the received digital data." Therefore, the clock

synchronization signals or "control signals" are included in the digital data that is received. Furthermore, col. 9, lines 11-13, of Chauvel disclose MPEG-2 audio and video decoders for receiving MPEG-2 audio and video transport streams associated with digital video broadcast signals (also see col. 3, lines 35-38 for MPEG standard). Chauvel clearly teaches receiving a transport stream associated with a digital video broadcast signal, the broadcast signal having data signals and control signals. The claimed step of generating a secondary set of control signals from the transport stream's control signals is met by the traffic controller 310 in Figure 1B. In further response the examiner also cites col. 12, lines 15-28, of Chauvel, in reference to the traffic controller 310 and circuit 200, where PACCLK high signals valid packet data and DERROR is used to indicate a packet that has data errors. Storing at least a portion of the transport stream data signals in a memory buffer controlled by the secondary set of control signals is met by memory interface 313 and buffer 312a in Figure 18B. In col. 10, lines 12-40, Chauvel discloses that, "The Transport Packet Parser (TPP) 210 in the circuit 200 processes the header of each packet and determines whether the packet should be discarded, further processed by ARM CPU 220, or if the packet contains relevant data and may be stored without any intervention from the ARM 220. The TPP 210 sends all packets requiring further processing or containing relevant data to the internal RAM 240 via the traffic controller (TC) 310...The data transfer from TPP 210 to SDRAM 312 is done via DMA [Direct Memory Access] set up by the traffic controller (TC) 310...The traffic controller 310 repacks the data and gets rid of the voids created by any header removal." Also, see Figs. 1B and 18B, where control signals indicated by the arrow between the traffic controller 310 and memory interface 313 indicate the claimed secondary set of control signals, and see col. 18, line 66 – col. 19, line 12, with reference to the

traffic controller authorizing and managing DMA transfers, memory access, data transfers, etc... Therefore, the traffic controller 310 is directly involved in storing at least a portion of the transport stream data signals in a memory buffer (312/312a, in Fig. 18B) *controlled by the secondary set of control signals* (which are output from the traffic controller 310 to the memory interface 313. Further, the step of sending the contents of the memory buffer to a system bus is met by memory 313 in Fig. 1B being sent through the traffic controller 310 to the system bus 330.

As to claim 18, the Chauvel et al reference discloses in Figure 1A a system for receiving a digital video broadcast signal comprising: a tuner 20 to receive a digital video broadcast signal (col. 8, lines 41-44 & col. 11, lines 1-2) and to provide an analog output signal (col. 8, lines 45-47); a demodulator as met by QPSK 30 to receive the output signal from the tuner and to provide a transport stream as shown in Fig. 1B where the transport data enters 210; and a video graphics adapter 200 (as shown in Figures 1A & 1B), which receives the transport stream and has a system interface port 210, the video graphics adapter further includes the claimed video engine 250 (Fig. 1B) and a video output port as shown in Fig. 1A coming out from item 200 as video output and is also shown in greater detail in Fig. 1B.

As to claim 19, the Chauvel et al reference further discloses in Figure 1B a system wherein the video graphics adapter 200 includes a memory 313 to store at least a portion of the data stream.

As to claim 20, the Chauvel et al reference further discloses in Figure 1B a central processing unit 220 (col. 9, lines 10-11) coupled (through the system bus 330) to the system

interface port 210 of the video graphics adapter 200; and in FIG. 17C a transport demultiplexor (decryption) coupled to a demodulator (QPSK).

11. Claim 21 is rejected under 35 U.S.C. 102(e) as being anticipated by Cheney et al (USPN 6,519,283), cited by the examiner.

As to claim 21, note the Cheney et al reference which discloses an integrated video processing system and method of storing video data. Cheney et al discloses multiple modes of operation (see col. 7, lines 27-37, col. 8, line 65 – col. 9, line 8 & lines 15-30). The claimed first mode of operation comprising storing pixel information in a frame buffer of a video adapter, wherein one line of frame buffer memory is representative of one line of a video image to be displayed is met by receiving an uncompressed signal from a second video source which may comprise either a digital signal or an analog signal (col. 6, lines 51-67 and/or 104 in Fig. 4), the pixel data (col. 4, lines 40-42 & 54-57 & col. 6, lines 26-34) is fetched and written to FIFO buffers and placed into frame buffers of the DRAM 52 in Fig. 2 (col. 5, line 52 – col. 6, line 6) and in one mode the uncompressed video is sent to a display. It is well known in the art of uncompressed video frame buffers that a line of frame buffer memory is *representative* of a line of a video image to be displayed. The claimed second mode of operation comprising storing compressed transport stream data in the frame buffer, wherein one line of frame buffer memory is representative of one transport stream packet is met by receiving an MPEG transport stream from a digital video source 101 in Fig 4 (col. 6, lines 35-44), the compressed MPEG transport steam (col. 5, lines 41-44) is sent from transport 103 to PCI bus 42/video decoder 106 (Figs. 2 & 4.) and is fetched and written to video FIFO buffer and placed into frame buffers of the DRAM 52 in Fig. 2 through memory controller 52 (col. 5, line 52 – col. 6, line 6) and in another mode of

operation the video is decompressed and sent to a display. It is well known in the art of video transport streams that are stored in frame buffers that a MPEG-2 transport stream packet has a fixed 188 byte length as defined by MPEG standards, and therefore, a line of frame buffer memory is *representative* of a transport stream packet since every MPEG-2 transport stream packet has already been produced and transmitted according to the established MPEG standards so that when received by a frame buffer memory a line of memory is representative of one transport stream packet.

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chauvel et al as applied to claim 14 above, in view of Cheney et al, both cited by the examiner.

As to claim 15, the Chauvel et al reference discloses the method of claim 14 wherein the steps of receiving, generating and storing occur in a mode of operation as described above in claim 14. Chauvel et al does not explicitly disclose multiple modes of operation, as well as, receiving a digital video signal that is of a different type than the transport stream. The Cheney reference discloses multiple modes of operation and a method of receiving a digital video signal that is of a different type than the transport stream, which is met by the video signals received at 104 in Fig. 4 (col. 4, lines 40-42 & 54-57 and col. 6, lines 62-67). The Cheney reference

discloses a first mode of operation as shown by receiving a digital video signal 101, which includes a MPEG transport stream (col. 6, lines 37-44). The Cheney reference also discloses another mode of operation where a digital video signal that is of a different type than the transport stream, which is met by the video signals received at 104 in Fig. 4 (col. 4, lines 40-42 & 54-57 and col. 6, lines 62-67) which includes data signals including pixel data signals and control signals which are met by the corresponding synchronization signals (col. 4, lines 56-57) and by "pixel select control" signals (col. 7, lines 40-41). The digital multi-standard decoder (DMSD) 105 provides synchronization signals, such as, horizontal sync and vertical sync and in addition, the memory controller 52 in Fig. 2 generates control signals to the DRAM 53 for storing video data in the frame buffer (col. 5, line 54 – col. 6, line 5). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Chauvel et al with the teachings of Cheney, so that a method comprising various modes of operation, including, receiving a transport stream associated with a digital video broadcast signal or receiving a digital video signal that is of a different type than the transport stream could be achieved.

As to claim 16, the Cheney reference as combined above, further discloses a camcorder or television camera may be used as an uncompressed signal and connected video cameras may inherently comprise the transmission of a zoom video signal (see col. 8, lines 24-25 and ZV port definition from the Microsoft Computer Dictionary, p. 586).

As to claim 17, the Chauvel et al reference further discloses a method wherein the memory buffer is a frame buffer as described in col. 8, line 15, in addition the Cheney et al

reference also discloses a method wherein the memory buffer is a frame buffer as shown in Fig. 2, DRAM 53 (col. 5, lines 65-67) and Fig. 6, element 653.

Allowable Subject Matter

14. Claims 2-13 and 22-23 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

As to claim 22, the prior art, alone or in combination, does not teach or fairly suggest a video graphics system comprising a data storage controller having at least one pair of a plurality of internal control ports to communicate control signals within the data storage controller.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

So, John Ling Wing (USPN 6,170,049) – Discloses PC systems and methods including the use of a PCI bus with MPEG transport stream and zoom video, as well as, frame buffer storage.

Hong, Xin Cheng (Simon) (USPN 5,943,064) – Discloses 2 modes of processing and display of video graphics pixel data.

Choi et al (USPN 6,285,408) – Discloses a digital audio/video system with multiple tuners.

Inoue et al (USPN 5,832,085) - Discloses a digital audio/video system with multiple tuners.

Miller et al (USPN 6,181,822) - Discloses a digital audio/video system with multiple tuners.

Jeon et al (USPN 5,926,228) - Discloses a digital audio/video system with multiple tuners and 2 modes.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael W. Hoye whose telephone number is (703) 305-6954. The examiner can normally be reached on Monday to Friday from 8:30 AM to 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Miller, can be reached at (703) 305-4795.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Michael W. Hoye
May 30, 2002

JOHN MILLER
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600